IPW

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449

Attorney Docket No.	Serial No.
2885/98	10/561,135
Applicant(s)	
VORBACH et al.	
Filing Date	**Group Art Unit**
April 25, 2006	2183

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	60/109,417	November 18, 1998	Jefferson et al.			
	RE34,444	November 16, 1993	Kaplinsky			
	RE37,195	May 29, 2001	Kean			
	4,414,547	November 8, 1983	Knapp et al.			
	4,571,736	February 18, 1986	Agrawal et al.			
	4,590,583	May 20, 1986	Miller			
	4,667,190	May 19, 1987	Fant et al.			
	4,686,386	August 11, 1987	Tadao			
	4,882,687	November 21, 1989	Gordon			
	4,884,231	November 28, 1989	Mor et al.			
	4,918,440	April 17, 1990	Furtek et al.			
	4,959,781	September 25, 1990	Rubenstein et al.			
	4,972,314	November 20, 1990	Getzinger et al.			
	5,010,401	April 23, 1991	Murakami et al.			
	5,034,914	July 23, 1991	Osterlund			
	5,041,924	August 20, 1991	Blackborow et al.			
	5,065,308	November 12, 1991	Evans			
	5,706,482	January 1998	Matsushima et al.			
	5,099,447	March 24, 1992	Myszewski			
	5,212,716	May 18, 1993	Ferraiolo et al.			
	5,218,302	June 8, 1993	Loewe et al.			
	5,237,686	August 17, 1993	Asano et al.			
	5,276,836	January 4, 1994	Fukumaru et al.			
	5,327,125	July 5, 1994	Iwase et al.			
	5,343,406	August 30, 1994	Freeman et al.			
	5,412,795	May 2, 1995	Larson			
	5,418,953	May 23, 1995	Hunt et al.			
	5,469,003	November 21, 1995	Kean			
	5,477,525	December 19, 1995	Masanobu Okabe			
	5,525,971	June 11, 1996	Flynn			
	5,537,580	July 16, 1996	Giomi et al.			
	5,550,782	August 27, 1996	Cliff et al.			
	5,581,731	December 3, 1996	King et al.			
	5,600,845	February 4, 1997	Gilson			
	5,625,836	April 29, 1997	Barker et al.			
	5,646,544	July 8, 1997	Iadanza			
	5,646,545	July 8, 1997	Trimberger et al.			
	5,675,757	October 7, 1997	Davidson et al.			

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/98	Serial No. 10/561,135
	Applicant(s) VORBACH et al.	
	Filing Date April 25, 2006	Group Art Unit 2183

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	5,694,602	December 2, 1997	Smith			
	5,737,565	April 7, 1998	Mayfield			
	5,745,734	April 28, 1998	Craft et al.			
	5,781,756	Jul 14, 1998	Hung			
	5,801,547	September 1, 1998	Kean			
	5,801,958	September 1, 1998	Dangelo et al.			
	5,815,715	September 29, 1998	Kayhan			
	5,815,726	September 29, 1998	Cliff			
	5,821,774	October 13, 1998	Veytsman et al.			
	5,831,448	November 3, 1998	Kean			
	5,844,422	December 1, 1998	Trimberger et al.			
	5,857,097	January 5, 1999	Henzinger et al.			
	5,860,119	January 12, 1999	Dockser			
	5,862,403	January 19, 1999	Kanai et al.			
	5,870,620	February 9, 1999	Kadosumi et al.			
	5,889,533	March 30, 1999	Lee			
	5,933,023	August 3, 1999	Young			
	5,960,193	September 28, 1999	Guttag et al.			
	5,966,143	October 12, 1999	Bretemitz, Jr.			
	5,978,583	November 2, 1999	Ekanadham et al.			
	5,999,990	December 7, 1999	Sharrit et al.			
	6,020,760	February 1, 2000	Sample et al.			
	6,026,481	February 15, 2000	New et al.			
	6,035,371	March 7, 2000	Magloire			
	6,044,030	Mar 28, 2000	Zheng et al.			
	6,055,619	April 25, 2000	North et al.			
	6,076,157	June 13, 2000	Borkenhagen et al.			
	6,077,315	June 20, 2000	Greenbaum et a.			
	6,084,429	July 4, 2000	Trimberger			
	6,105,106	August 15, 2000	Manning			
	6,118,724	September 12, 2000	Higginbottom			
	6,134,166	October 17, 2000	Lytle et al.			
	6,137,307	October 24, 2000	Iwanczuk et al.			
	6,154,048	November 28, 2000	Iwanczuk et al.			
	6,154,049	November 28, 2000	New			
	6,157,214	December 5, 2000	Marshall			
	6,185,256	February 6, 2001	Saito et al.			
	6,185,731	February 6, 2001	Maeda et al.			
	6,188,240	February 13, 2001	Nakaya			

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/98	Serial No. 10/561,135
	Applicant(s) VORBACH et al.	
	Filing Date April 25, 2006	Group Art Unit 2183

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	6,188,650	February 13, 2001	Hamada et al.			
	6,198,304	March 6, 2001	Sasaki			
	6,201,406	March 13, 2001	Iwanczuk et al.			
	6,204,687	March 20, 2001	Schultz et al.			
	6,215,326	April 10, 2001	Jefferson et al.			
	6,216,223	April 10, 2001	Revilla et al.			
	6,247,147	June 12, 2001	Beenstra et al.			
	6,252,792	June 26, 2001	Marshall et al.			
	6,256,724	July 3, 2001	Hocevar et al.			
	6,262,908	July 17, 2001	Marshall et al.			
	6,266,760	July 24, 2001	DeHon et al.			
	6,285,624	September 4, 2001	Chen			
	6,311,265	October 30, 2001	Beckerle et al.			
	6,353,841	March 5, 2002	Marshall et al.			
	6,362,650	Mar 26, 2002	New et al.			
	6,373,779	April 16, 2002	Pang et al.			
	6,374,286	April 16, 2002	Gee			
	6,381,624	April 30, 2002	Colon-Bonet et al.			
	6,400,601	June 4, 2002	Sudo et al.			
	6,421,808	July 16, 2002	McGeer			
	6,426,649	July 30, 2002	Fu et al.			
	6,427,156	July 30, 2002	Chapman et al.			
	6,430,309	August 6, 2002	Pressman et al.			
	6,434,642	August 13, 2002	Camilleri et al.			
	6,438,747	August 20, 2002	Schreiber et al.			
	6,476,634	November 5, 2002	Bilski			
	6,483,343	November 19, 2002	Faith et al.			
	6,487,709	November 26, 2002	Keller et al.			
	6,507,898	January 14, 2003	Gibson et al.			
	6,507,947	January 14, 2003	Schreiber et al.			
	6,516,382	February 4, 2003	Manning			
	6,518,787	February 11, 2003	Allegrucci et al.			
	6,523,107	February 18, 2003	Stansfield et al.			
	6,525,678	February 25, 2003	Veenstra et al.			
	6,538,470	March 25, 2003	Langhammer et al.			
	6,539,415	March 25, 2003	Mercs			
	6,539,438	March 25, 2003	Ledzius et al.			

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/98	Serial No. 10/561,135
	Applicant(s) VORBACH et al.	
	Filing Date April 25, 2006	Group Art Unit 2183

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	6,542,394	April 1, 2003	Marshall et al.			
	6,553,395	April 22, 2003	Marshall et al.			
	6,567,834	May 20, 2003	Marshall et al.			
	6,631,487	October 7, 2003	Abramovici et al.			
	6,633,181	October 14, 2003	Rupp			
	6,658,564	December 2, 2003	Smith et al.			
	6,665,758	December 16, 2003	Frazier et al.			
	6,708,325	March 16, 2004	Cooke et al.			
	6,748,440	June 8, 2004	Lisitsa et al.			
	6,754,805	June 22, 2004	Yujen Juan			
	6,757,892	June 29, 2004	Gokhale et al.			
	6,782,445	August 24, 2004	Olgiati et al.			
	6,802,026	October 5, 2004	Patterson et al.			
	6,803,787	October 12, 2004	Wicker, Jr.			
	6,820,188	November 16, 2004	Stansfield et al.			
	6,829,697	December 7, 2004	Davis et al.			
	6,847,370	January 25, 2005	Baldwin et al.			
	6,871,341	March 22, 2005	Shyr			
	6,874,108	March 29, 2005	Abramovici et al.			
	6,886,092	April 26, 2005	Douglass et al.			
	6,901,502	May 31, 2005	Yano et al.			
	6,928,523	August 9, 2005	Yamada, Akira			
	6,977,649	December 20, 2005	Baldwin et al.			
	7,000,161	February 14, 2006	Allen et al.			
	7,007,096	February 28, 2006	Lisitsa et al.			
	7,010,687	March 7, 2006	Ichimura			
	7,038,952	May 2, 2006	Zack et al.			
	7,043,416	**May 9, 2006**	**Lin**			
	7,210,129	April 24, 2007	May et al.			
	7,237,087	June 26, 2007	Vorbach et al.			
	7,249,351	July 24, 2007	Songer et al.			
	7,254,649	August 7, 2007	Subramanian et al.			
	7,340,596	March 4, 2008	Crosland et al.			

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/98	Serial No. 10/561,135
	Applicant(s) VORBACH et al.	
	Filing Date April 25, 2006	Group Art Unit 2183

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	7,346,644	March 18, 2008	Langhammer et al.			
	7,350,178	March 25, 2008	Crosland et al.			
	2001/001860	May 24, 2001	Bieu			
	2001/ 018733	October 18, 2001	Fujii et al.			
	2001/032305	January 31, 2002	Barry			
	2002/103839	August 1, 2002	Ozawa			
	2002/124238	September 5, 2002	Metzgen			
	2002/138716	September 26, 2002	Master et al.			
	2003/001615	January 2, 2003	Sueyoshi et al.			
	2003/061542	March 27, 2003	Bates et al.			
	2003/062922	April 3, 2003	Douglass et al.			
	2003/086300	May 8, 2003	Noyes et al.			
	2004/0078548	April 22, 2004	Claydon et al.			
	2005/066213	March 24, 2005	Vorbach et al.			
	2005/144210	June 30, 2005	Simkins et al.			
	2005/144212	June 30, 2005	Simkins et al.			
	2005/144215	June 30, 2005	Simkins et al.			
	2006/230094	October 12, 2006	Simkins et al.			
	2006/230096	October 12, 2006	Thendean et al.			
	2009/0085603	April 2, 2009	Paul et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
	0 398 552	November 22, 1990	EPO				
	0 696 001	February 7, 1996	EPO				
	0 746 106	December 4, 1996	EPO				
	1 061 439	December 20, 2000	EPO				
	1 115 204	July 11, 2001	EPO				
	1 669 885	June 14, 2006	EPO			Abstract	
	2 752 466	February 20, 1998	France			English equivalent: USP 6,425,054	
	44 16 881	November 17, 1994	Germany			Abstract	
	198 22 776	March 25, 1999	Germany			Abstract	
	2 304 438	March 19, 1997	United Kingdom				
	WO98/010517	March 12, 1998	PCT				
	WO98/035294	August 13, 1998	PCT				

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/98	Serial No. 10/561,135
	Applicant(s) VORBACH et al.	
	Filing Date April 25, 2006	Group Art Unit 2183

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
	WO00/045282	August 3, 2000	PCT				
	WO00/049496	August 24, 2000	PCT				
	WO02/050665	June 27, 2002	PCT				
	WO 03/091875	November 6, 2003	PCT				
	WO04/053718	June 24, 2004	PCT				
	WO05/045692	May 19, 2005	PCT				
	1-229378	September 13, 1989	Japan			Abstract	
	5-509184	December 16, 1993	Japan			English Equivalent: USP 5,193,202	
	6-266605	September 22, 1994	Japan			Abstract	
	7-086921	March 31, 1995	Japan			Abstract	
	8-069447	March 12, 1996	Japan			Abstract	
	8-101761	April 16, 1996	Japan			Abstract	
	8-102492	April 16, 1996	Japan			Abtstract	
	8-148989	June 7, 1995	Japan			Abstract	
	8-221164	August 30, 1996	Japan			Abstract	
	9-294069	November 11, 1997	Japan			Abstract	
	2000-076066	March 14, 2000	Japan			Abstract	
	2000-181566	June 30, 2000	Japan			Computer Translation	
	2000-201066	July 18, 2000	Japan			Abstract	
	2000-311156	November 7, 2000	Japan			Abstract	
	2001-500682	January 16, 2001	Japan			Abstract	

OTHER DOCUMENTS

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Abnous et al., "Ultra-Low-Power Domain-Specific Multimedia Processors," U.C. Berkeley, 1996 IEEE, pp. 461-470.
	Ade, et al., "Minimum Memory Buffers in DSP Applications," Electronics Letters, vol. 30, No. 6, March 17, 1994, pp. 469-471.
	Advanced RISC Machines, "Introduction to AMBA," October 1996, Section 1, pp. 1-7.
	ARM, "The Architecture for the Digital World," http://www.arm.com/products/ March 18, 2009, 3 pages.
	ARM, "The Architecture for the Digital World; Milestones," http://www.arm.com/aboutarm/milestones.html March 18, 2009, 5 pages.
	Albaharna, O.T. et al., "On the Viability of FPGA-Based Integrated Coprocessors," Dept. of Electrical and Electronic Engineering, Imperial College of Science, London, 1999 IEEE, pp. 206-215.
	Altera, "Flex 8000 Programmable Logic Device Family," Altera Corporation product description, January 2003, pp. 1-62.
	Altera, "Flex 10K Embedded Programmable Logic Device Family," Altera Corporation product description, January 2003, pp. 1-128.
	Asari, K. et al., "FeRAM circuit technology for system on a chip," *Proceedings First NASA/DoD Workshop on Evolvable Hardware* (1999), pp. 193-197.
	Athanas et al., "Processor Reconfiguration Through Instruction-Set Metamorphosis," 1993, IEEE Computers, pp. 11-18.
	Atmel, 5-K-50K Gates Coprocessor FPGA with Free Ram, Data Sheet, July 2006, 55 pages.

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/98	Serial No. 10/561,135
	Applicant(s) VORBACH et al.	
	Filing Date April 25, 2006	Group Art Unit 2183

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Atmel, FPGA-based FIR Filter Application Note, September 1999, 10 pages.
	Atmel, "An Introduction to DSP Applications using the AT40K FPGA," FPGA Application Engineering, San Jose, CA, April 2004, 15 pages.
	Atmel, Configurable Logic Design & Application Book, Atmel Corporation, 1995, pp. 2-19 through 2-25.
	Atmel, Field Programmable Gate Array Configuration Guide, AT6000 Series Configuration Data Sheet, September 1999, pp. 1-20.
	Bacon, D. et al., "Compiler Transformations for High-Performance Computing," ACM Computing Surveys, 26(4):325-420 (1994).
	Bakkes, P.J., et al., "Mixing Fixed and Reconfigurable Logic for Array Processing," Dept. of Electrical and Electronic Engineering, University of Stellenbosch, South Africa, 1996 IEEE, pp. 118-125.
	Becker, J. et al., "Architecture, Memory and Interface Technology Integration of an Industrial/Academic Configurable System-on-Chip (CSoC)," IEEE Computer Society Annual Workshop on VLSI (WVLSI 2003), (February 2003).
	Becker, J., "Configurable Systems-on-Chip (CSoC)," (Invited Tutorial), Proc. of 9th Proc. of XV Brazilian Symposium on Integrated Circuit, Design (SBCCI 2002), (September 2002).
	Becker et al., "Automatic Parallelism Exploitation for FPL-Based Accelerators," 1998, Proc. 31st Annual Hawaii International Conference on System Sciences, pp. 169-178.
	Bratt, A, "Motorola field programmable analogue arrays, present hardware and future trends," Motorola Programmable Technology Centre, Gadbrook Business Centre, Northwich, Cheshire, 1998, The Institute of Electrical Engineers, IEE. Savoy Place, London, pp. 1-5.
	Cardoso, J.M.P., et al., "A novel algorithm combining temporal partitioning and sharing of functional units," University of Algarve, Faro, Portugal, 2001 IEEE, pp. 1-10.
	Cardoso, J.M.P., et al., "Compilation and Temporal Partitioning for a Coarse-Grain Reconfigurable Architecture," New Algorithms, Architectures and Applications for Reconfigurable Computing, LYSACHT, P. & ROSENTIEL, W. eds., (2005) pp. 105-115.
	Cardoso, J.M.P., et al., "Macro-Based Hardware Compilation of Java™ Bytecodes into a Dynamic Reconfigurable Computing System," Field-Programmable Custom Computing Machines (1999) FCCM '99. Proceedings. Seventh Annual IEEE Symposium on NAPA Valley, CA, USA, 21-23 April 1999, IEEE Comput. Soc, US, (21 April 1999) pp.2-11.
	Chaudhry, G.M. et al., "Separated caches and buses for multiprocessor system," Circuits and Systems, 1993; Proceedings of the 36th Midwest Symposium on Detroit, MI, USA, 16-18 August 1993, New York, NY IEEE, 16 August 1993, Pages 1113-1116, XP010119918 ISBN: 0-7803-1760-2.
	Clearspeed, CSX Processor Architecture, Whitepaper, PN-1110-0702, 2007, pp. 1-15, www.clearspeed.com.
	Clearspeed, CSX Processor Architecture, Whitepaper, PN-1110-0306, 2006, pp. 1-14, www.clearspeed.com.
	Compton, K., et al., "Configurable Computing: A Survey of Systems and Software," Northwestern University, Dept. of ECE, Technical Report, 1999, (XP-002315148), 39 pages.
	Cook, Jeffrey J., "The Amalgam Compiler Infrastructure," Thesis at the University of Illinois at Urbana-Champaign (2004) Chapter 7 & Appendix G.
	Cronquist, D., et al., 'Architecture Design of Reconfigurable Pipelined Datapaths," Department of Computer Science and Engineering, University of Washington, Seattle, WA, Proceedings of the 20th Anniversary Conference on Advanced Research in VSLI, 1999, pp. 1-15.
	Culler, D.E; Singh, J.P., "Parallel Computer Architecture," Pages 434-437, 1999, Morgan Kaufmann, San Francisco, CA USA, XP002477559.
	DeHon, Andre, "Reconfigurable Architectures for General-Purpose Computing," Massachusetts Institute of Technology, Technical Report AITR-1586, October 1996 (1996-10), XP002445054, Cambridge, MA, pp. 1-353.
	Del Corso et al., "Microcomputer Buses and Links," Academic Press Inc. Ltd., 1986, pp. 138-143, 277-285.
	Diniz, P., et al., "A behavioral synthesis estimation interface for configurable computing," University of Southern California, Marina Del Rey, CA, 2001 IEEE, pp. 1-2.
	Ebeling, C., et al., "Mapping Applications to the RaPiD Configurable Architecture," Department of Computer Science and Engineering, University of Washington, Seattle, WA, FPGAs for Custom Computing Machines, 1997. Proceedings., The 5th Annual IEEE Symposium, Publication Date: 16-18 Apr 1997, 10 pages.

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/98	Serial No. 10/561,135
	Applicant(s) VORBACH et al.	
	Filing Date April 25, 2006	Group Art Unit 2183

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Equator, Pixels to Packets, Enabling Multi-Format High Definition Video, Equator Technologies BSP-15 Product Brief, www.equator.com, 2001, 4 pages.
	Fawcett, B.K., "Map, Place and Route: The Key to High-Density PLD Implementation," Wescon Conference, IEEE Center (7 November 1995) pp. 292-297.
	Freescale Slide Presentation, An Introduction to Motorola's RCF (Reconfigurable Compute Fabric) Technology, Presented by Frank David, Launched by Freescale Semiconductor, Inc., 2004, 39 pages.
	Genius, D., et al., "A Case for Array Merging in Memory Hierarchies," Proceedings of the 9th International Workshop on Compilers for Parallel Computers, CPC'01 (June 2001), 10 pages.
	Hartenstein, R. et al., "A new FPGA architecture for word-oriented datapaths," Proc. FPL'94, Springer LNCS, September 1994, pp. 144-155.
	Hendrich, N., et al., "Silicon Compilation and Rapid Prototyping of Microprogrammed VLSI-Circuits with MIMOLA and SOLO 1400," Microprocessing & Microprogramming (September 1992) vol. 35(1-5), pp. 287-294.
	Hwang, K., "Advanced Computer Architecture – Parallelism, Scalability, Programmability," 1993, McGraw-Hill, Inc., pp. 348-355.
	Hwang, K., "Computer Architecture and Parallel Processing," Data Flow Computers and VLSI Computations, XP-002418655, 1985 McGraw-Hill, Chapter 10, pp. 732-807.
	IBM Technical Disclosure Bulletin, IBM Corp., New York, XP000424878, Bd. 36, Nr. 11, 1 November 1993, pp. 335-336.
	"IEEE Standard Test Access Port and Boundary-Scan Architecture," IEEE Std. 1149.1-1990, 1993, pp. 1-127.
	Inside DSP, "Ambric Discloses Massively Parallel Architecture," August 23, 2006, http://www.insidedsp.com/Articles/tabid/64/articleType/ArticleView/articleId/155/Default.aspx, 2 pages.
	Intel, Intel MXP5800/MXP5400 Digital Media Processors, Architecture Overview, June 2004, Revision 2.4, pp. 1-24.
	Jantsch, Axel et al., "Hardware/Software Partitioning and Minimizing Memory Interface Traffic," Electronic System Design Laboratory, Royal Institute of Technology, ESDLab, Electrum 229, S-16440 Kista, Sweden (April 1994), pp. 226-231.
	Kaul, M., et al., "An automated temporal partitioning and loop fission approach of FPGA based reconfigurable synthesis of DSP applications," University of Cincinnati, Cincinnati, OH, ACM 1999, pp. 616-622.
	Kean, T.A., "Configurable Logic: A Dynamically Programmable Cellular Architecture and its VLSI Implementation," University of Edinburgh (Dissertation) 1988, pp. 1-286
	Kean, T., et al., "A Fast Constant Coefficient Multiplier for the XC6200," Xilinx, Inc., Lecture Notes in Computer Science, Vol. 1142, Proceedings of the 6th International Workshop of Field-Programmable Logic, 1996, 7 pages.
	Kim et al., "A Reconfigurable Multifunction Computing Cache Architecture," IEEE Transactions on Very Large Scale Integration (VLSI) Systems Volume 9, Issue 4, Aug 2001 Page(s):509 – 523.
	Knittel, Gunter, "A PCI-compatible FPGA-Coprocessor for 2D/3D Image Processing," University of Turgingen, Germany, 1996 IEEE, pp. 136-145.
	Koch, Andreas et al., "High-Level-Language Compilation for Reconfigurable Computers," Proceedings of European Workshop on Reconfigurable Communication-Centric SOCS (June 2005) 8 pages.
	Lange, H. et al., "Memory access schemes for configurable processors," Field-Programmable Logic and Applications, International Workshop, FPL, 27 August 2000, pages 615-625, XP02283963.
	Larsen, S., et al., "Increasing and Detecting Memory Address Congruence," Proceedings of the 2002 IEEE International Conference on Parallel Architectures and Compilation Techniques (PACT'02), pp. 1-12 (September 2002).
	Lee, Ming-Hau et al., "Designs and Implementation of the MorphoSys Reconfigurable Computing Processors," The Journal of VLSI Signal Processing, Kluwer Academic Publishers, BO, Vol. 24, No. 2-3, 2 March 2000, pp. 1-29.
	Lee et al., "A new distribution network based on controlled switching elements and its applications," IEEE/ACT Trans. of Networking, Vol. 3, No. 1, pp. 70-81, February 1995.
	Lee, R. B., et al., "Multimedia extensions for general-purpose processors," *IEEE Workshop on Signal Processing Systems, SIPS 97 – Design and Implementation* (1997), pp. 9-23.
	Margolus, N., "An FPGA architecture for DRAM-based systolic computations," Boston University Center for Computational Science and MIT Artificial Intelligence Laboratory, IEEE 1997, pp. 2-11.
	Mei, Bingfeng, "A Coarse-Grained Reconfigurable Architecture Template and Its Compilation Techniques," Katholeike Universiteit Leuven, PhD Thesis, January 2005, IMEC vzw, Universitair Micro-Electronica Centrum, Belgium, pp. 1-195 (and Table of Contents).

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/98	Serial No. 10/561,135
	Applicant(s) VORBACH et al.	
	Filing Date April 25, 2006	Group Art Unit 2183

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Mei, Bingfeng et al., "Design and Optimization of Dynamically Reconfigurable Embedded Systems," IMEC vzw, 2003, Belgium, 7 pages, http://www.imec.be/reconfigurable/pdf/ICERSA_01_design.pdf.
	Mei, Bingfeng et al., "Adres: An Architecture with Tightly Coupled VLIW Processor and Coarse-Grained Reconfigurable Matrix," Proc. *Field-Programmable Logic and Applications* (FPL 03), Springer, 2003, pp. 61-70.
	Miyamori, T., et al., "REMARC: Reconfigurable Multimedia Array Coprocessor," Computer Systems Laboratory, Stanford University, IEICE TRANSACTIONS ON INFORMATION AND SYSTEMS E SERIES D, 1999; (abstract): Proceedings of the 1998 ACM/SIGDA sixth international symposium on Field programmable gate arrays, p.261, February 22-25, 1998, Monterey, California, United States, pp. 1-12.
	Moraes, F., et al., "A Physical Synthesis Design Flow Based on Virtual Components," XV Conference on Design of Circuits and Integrated Systems (November 2000) 6 pages.
	Muchnick, S., "Advanced Compiler Design and Implementation," (Morgan Kaufmann 1997), Table of Contents, 11 pages.
	Murphy, C., "Virtual Hardware Using Dynamic Reconfigurable Field Programmable Gate Arrays," Engineering Development Centre, Liverpool John Moores University, UK, GERI Annual Research Symposium 2005, 8 pages.
	Nageldinger, U., "Design-Space Exploration for Coarse Grained Reconfigurable Architectures," (Dissertation) Universitaet Kaiserslautern, 2000, Chapter 2, pp. 19-45.
	Neumann, T., et al., "A Generic Library for Adaptive Computing Environments," Field Programmable Logic and Applications, 11th International Conference, FPL 2001, Proceedings (Lecture Notes in Computer Science, vol. 2147) (2001) pp. 503-512.
	Olukotun, K., "The Case for a Single-Chip Microprocessor," ACM Sigplan Notices, ACM, Association for Computing Machinery, New York, Vol. 31, No. 9, September 1996 (1996-09-00) pp. 2-11.
	PACT Corporation, "The XPP Communication System," Technical Report 15 (2000), pp. 1-16.
	Parhami, B., "Parallel Counters for Signed Binary Signals," Signals, Systems and Computers, 1989, Twenty-Third Asilomar Conference, Volume 1, pp. 513-516.
	PCI Local Bus Specification, Production Version, Revision 2.1, June 1, Portland, OR, 1995, pp. 1-281.
	Piotrowski, A., "IEC-BUS, Die Funktionsweise des IEC-Bus unde seine Anwendung in Geräten und Systemen," 1987, Franzis-Verlag GmbH, München, pp. 20-25. **[ENGLISH ABSTRACT INCLUDED]**
	Pirsch, P. et al., "VLSI implementations of image and video multimedia processing systems," *IEEE Transactions on Circuits and Systems for Video Technology*, vol. 8, no. 7, Nov. 1998, pp. 878-891.
	Quenot, G.M., et al., "A Reconfigurable Compute Engine for Real-Time Vision Automata Prototyping," Laboratoire Systeme de Perception, DGA/Etablissement Technique Central de l'Armement, France, 1994 IEEE, pp. 91-100.
	Ryo, A., "Auszug aus Handbuch der Informationsverarbeitung," ed. Information Processing Society of Japan, *Information Processing Handbook, New Edition*, Software Information Center, Ohmsha, December 1998, 4 pages. [Translation provided]
	Saleeba, Z.M.G., "A Self-Reconfiguring Computer System," Department of Computer Science, Monash University (Dissertation) 1998, pp. 1-306.
	Salefski, B. et al., "Re-configurable computing in wireless," *Annual ACM IEEE Design Automation Conference: Proceedings of the 38th conference on Design automation* (2001) pp. 178-183.
	Schmidt, H. et al., "Behavioral synthesis for FGPA-based computing," Carnegie Mellon University, Pittsburgh, PA, 1994 IEEE, pp. 125-132.
	Schmidt, U. et al., "Datawave: A Single-Chip Multiprocessor for Video Applications," *IEEE Micro*, vol. 11, no. 3, May/June 1991, pp. 22-25, 88-94.
	Schönfeld, M., et al., "The LISA Design Environment for the Synthesis of Array Processors Including Memories for the Data Transfer and Fault Tolerance by Reconfiguration and Coding Techniques," J. VLSI Signal Processing Systems for Signal, Image, and Video Technology, (1 October 1995) vol. 11(1/2), pp. 51-74.
	Shin, D., et al., "C-based Interactive RTL Design Methodology," Technical Report CECS-03-42 (December 2003) pp. 1-16.
	Singh, H. et al., "MorphoSys: An Integrated Reconfigurable System for Data-Parallel Computation-Intensive Applications," University of California, Irvine, CA. and Federal University of Rio de Janeiro, Brazil, 2000, IEEE Transactions on Computers, pp. 1-35.
	Sondervan, J., "Retiming and logic synthesis," Electronic Engineering (January 1993) vol. 65(793), pp. 33, 35-36.
	Soni, M., "VLSI Implementation of a Wormhole Run-time Reconfigurable Processor," June 2001, (Masters Thesis)Virginia Polytechnic Institute and State University, 88 pages.

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/98	Serial No. 10/561,135
	Applicant(s) VORBACH et al.	
	Filing Date April 25, 2006	Group Art Unit 2183

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Sutton et al., "A Multiprocessor DSP System Using PADDI-2," U.C. Berkeley, 1998 ACM, pp. 62-65.
	Tsutsui, A., et al., "YARDS: FPGA/MPU Hybrid Architecture for Telecommunication Data Processing," NTT Optical Network Systems Laboratories, Japan, 1997 ACM, pp. 93-99.
	Vasell et al., "The Function Processor: A Data-Driven Processor Array for Irregular Computations," Chalmers University of Technology, Sweden, 1992, pp. 1-21.
	Waingold, E., et al., "Baring it all to software: Raw machines," IEEE Computer, September 1997, at 86-93.
	Weinhardt, Markus et al., "Memory Access Optimization for Reconfigurable Systems," IEEE Proceedings Computers and Digital Techniques, 48(3) (May 2001) pp. 1-16.
	Wolfe, M. et al., "High Performance Compilers for Parallel Computing," (Addison-Wesley 1996) Table of Contents, 11 pages.
	Wu, et al., "A New Cache Directory Scheme," IEEE, pp. 466-472, June 1996.
	XILINX, "The Programmable Logic Data Book," 1994, Section 2, pp.1-231, Section 8, pp. 1, 23-25, 29, 45-52, 169-172.
	XILINX, "Spartan and SpartanXL Families Field Programmable Gate Arrays," January 1999, Xilinx, pp. 4-3 through 4-70.
	XILINX, "XC6200 Field Programmable Gate Arrays," April 24, 1997, Xilinx product description, pp. 1-73.
	XILINX, "XC3000 Series Field Programmable Gate Arrays," November 6, 1998, Xilinx product description, pp. 1-76.
	XILINX, "XC4000E and XC4000X Series Field Programmable Gate Arrays," May 14, 1999, Xilinx product description, pp. 1-68.
	XILINX, "Virtex-E 1.8 V Extended Memory Field Programmable Gate Arrays," July 17, 2002, Xilinx Production Product Specification, pp. 1-118.
	XILINX, "Virtex-II and Virtex-II Pro X FPGA User Guide," March 28, 2007, Xilinx user guide, pp. 1-559.
	Xu, H. et al., "Parallel QR Factorization on a Block Data Flow Architecture," Conference Proceeding Article, March 1, 1992, pages 332-336 XPO10255276, page 333, Abstract 2.2, 2.3, 2.4 - page 334.
	Zhang, et al., "A 1-V Heterogeneous Reconfigurable DSP IC for Wireless Baseband Digital Signal Processing," IEEE Journal of Solid-State Circuits, Vol. 35, No. 11, November 2000, pp. 1697-1704.
	Zhang et al., "Abstract: Low-Power Heterogeneous Reconfigurable Digital Signal Processors with Energy-Efficient Interconnect Network," U.C. Berkeley (2004), pp. 1-120.
	Zima, H. et al., "Supercompilers for parallel and vector computers," (Addison-Wesley 1991) Table of Contents, 5 pages.

EXAMINER	DATE CONSIDERED
EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	